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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	§	Docket No. **AT9-98-781**
ARIMILLI ET AL.	§	
Serial No. **09/340,074**	§	Examiner: **TZENG, F.**
Filed: **25 JUNE 1999**	§	Art Unit: **2651**
For: **LAYERED LOCAL CACHE WITH LOWER LEVEL CACHE OPTIMIZING ALLOCATION MECHANISM**	§	

REPLY BRIEF

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

This Reply Brief is submitted in answer to the Examiner's Answer dated March 22, 2002.

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service on the below date with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D. C. 20231.

5/21/02
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ARGUMENT

In the Appeal Brief filed October 23, 2001, Appellants argued that col. 3, lines 5-10 of U.S. Patent No. 5,737,751 to *Patel et al.* (*Patel*), which were relied upon by the Examiner in the Final Rejection, do not disclose the claimed step and means for selecting a victim cache block in a lower level cache (see, e.g., Claim 1, lines 7-8 and Claim 11, lines 9-12) as required for a rejection under 35 U.S.C. § 102 or § 103. In apparent acquiescence to Appellants' position, the Examiner, in paragraph 11 of the Examiner's Answer dated March 22, 2002, fails to respond the Appellants arguments. Instead, the Examiner shifts positions and now relies upon col. 6, lines 59-67, col. 7, lines 1-13, and col. 2, lines 42-45 of *Patel* as teaching the claimed step and means for selecting a victim cache block in a lower level cache "based at least in part on cache hits in the upper level cache" as demonstrated below.

As pointed out by the Examiner at page 7 of the Examiner's Answer, col. 6, lines 59-67 and col. 7, lines 1-13 teach that a memory access miss in the level-one (L1) cache will result in an access to the level-two (L2) cache. The Examiner then points out that col. 2, lines 42-45 of *Patel* teach weak inclusion between the L1 and L2 caches, meaning that "changes to the L1 cache are updated in the L2 cache periodically using write-back operations" (*Patel*, col. 2, lines 43-45). Although not expressed in the Examiner's Answer, the implication of the Examiner's reliance upon these two passages is that the L2 cache hits generated by the write-back operations are reflected in a conventional LRU algorithm (*Patel*, col. 2, lines 14-19) and that the selection of a victim cache block in the L2 cache utilizing the conventional LRU algorithm is therefore "based at least in part on cache hits in the upper level cache" as claimed.

Appellants respectfully traverse the Examiner's position because the write-back updates to the L2 cache now relied upon by the Examiner result in L2 cache hits being reflected in the L2 victim selection (i.e., LRU) algorithm rather than L1 cache hits (i.e., "cache hits in the upper level cache") as required by the present claims. While it is true that certain access requests will generate hits or misses in both the L1 and L2 caches, *Patel's* conventional LRU algorithm, unlike the claimed

invention, takes into account only activity within the L2 cache rather than cache hit information from the L1 cache.

Appellants further point out that the Examiner's proposed construction of "cache hits in the upper level cache" as including write-back hits in the L2 cache is precluded by the present specification and claims. In particular, exemplary Claim 1 and similar Claim 11 are both written in the "means or step for" format provided for in § 112, paragraph 6, thus requiring the claim terminology to be construed by reference to the "structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112, paragraph 6 (see also, *In re Donaldson*, 16 F.3d 1189, 29 USPQ2s 1845 (Fed. Cir. 1994)(*en banc*)).

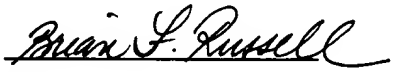
In the present case, the present specification and Figure 4 disclose that L2 controller 214 receives a flag indicating the hit/miss status of L1 cache 200 for every cache access request (page 20, lines 1-5). These hit/miss flags are utilized by L2 controller 214 to maintain a hybrid L2 LRU 232, "which includes information based on not only L1 misses, but further on L1 hits. L2 victim select logic 234 uses the information from hybrid L2 LRU 232" to select a victim cache line for replacement in L2 cache 202 (page 22, lines 4-7). Thus, when the claimed step and means for "selecting a victim cache block in the lower level cache ... based at least in part on cache hits in the upper level cache" is construed by reference to the present specification in accordance with § 112, paragraph 6, the claimed step and means must be understood as employing actual hit information from the L1 cache within the L2 victim selection algorithm. Because *Patel* does not disclose any similar or equivalent structure, material, or acts that permit the L2 victim selection based upon cache hit information from the L1 cache, but instead discloses a conventional LRU that selects a victim cache block based on hits and misses in the L2 cache alone, *Patel* does not render the present claims unpatentable under 35 U.S.C. § 102 or § 103.

Moreover, the Examiner's proposed construction of L2 write-back cache hits as L1 cache hits is improper because it violates the doctrine of claim differentiation. "Under the doctrine of claim differentiation, it is presumed that different words used in different claims result in a difference in

meaning and scope for each of the claims." *Clearstream Wastewater Systems, Inc. v. Hydro-Action, Inc.*, 206 F.3d 1440, 54 USPQ2d 1185 (Fed. Cir. 2000). In the present case, Claim 2, which depends from exemplary Claim 1, further refines the invention recited in Claim 1, stating "the victim cache block is further selected based in part of the cache activity of the lower level cache." If *Patel's* L2 cache hits are considered L1 cache hits as urged by the Examiner, then the "cache activity of the lower level cache" recited in Claim 2 would not have any substantial difference in meaning from the "cache hits in the upper level cache" recited in Claim 1. In addition, if the Examiner's claim construction were adopted, Claim 2 would have the same scope as Claim 1, again contrary to the doctrine of claim differentiation. Consequently, the doctrine of claim differentiation mandates the rejection of the Examiner's claim construction and the reversal of the rejection of the present claims in view of *Patel*.

In the foregoing argument, Appellants have demonstrated that *Patel* does not disclose the claimed step and means for selecting a victim cache block in a lower level cache and therefore respectfully request that the Board to reverse the rejection of the claims.

Respectfully submitted,



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